ESF II project of the University of West Bohemia in Pilsen

reg. number: CZ.02.2.69/0.0/0.0/18_056/0013239

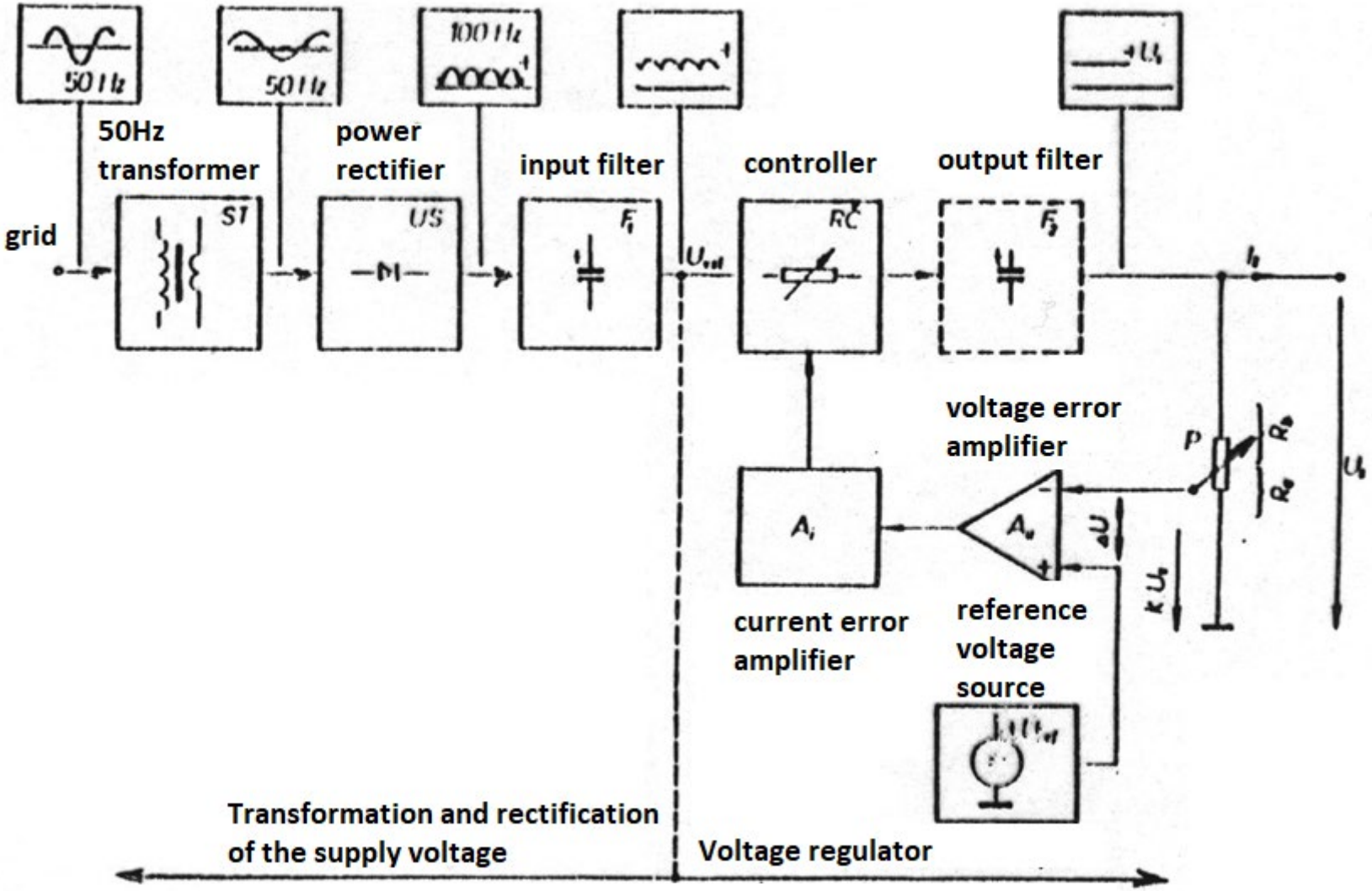
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Linear regulators

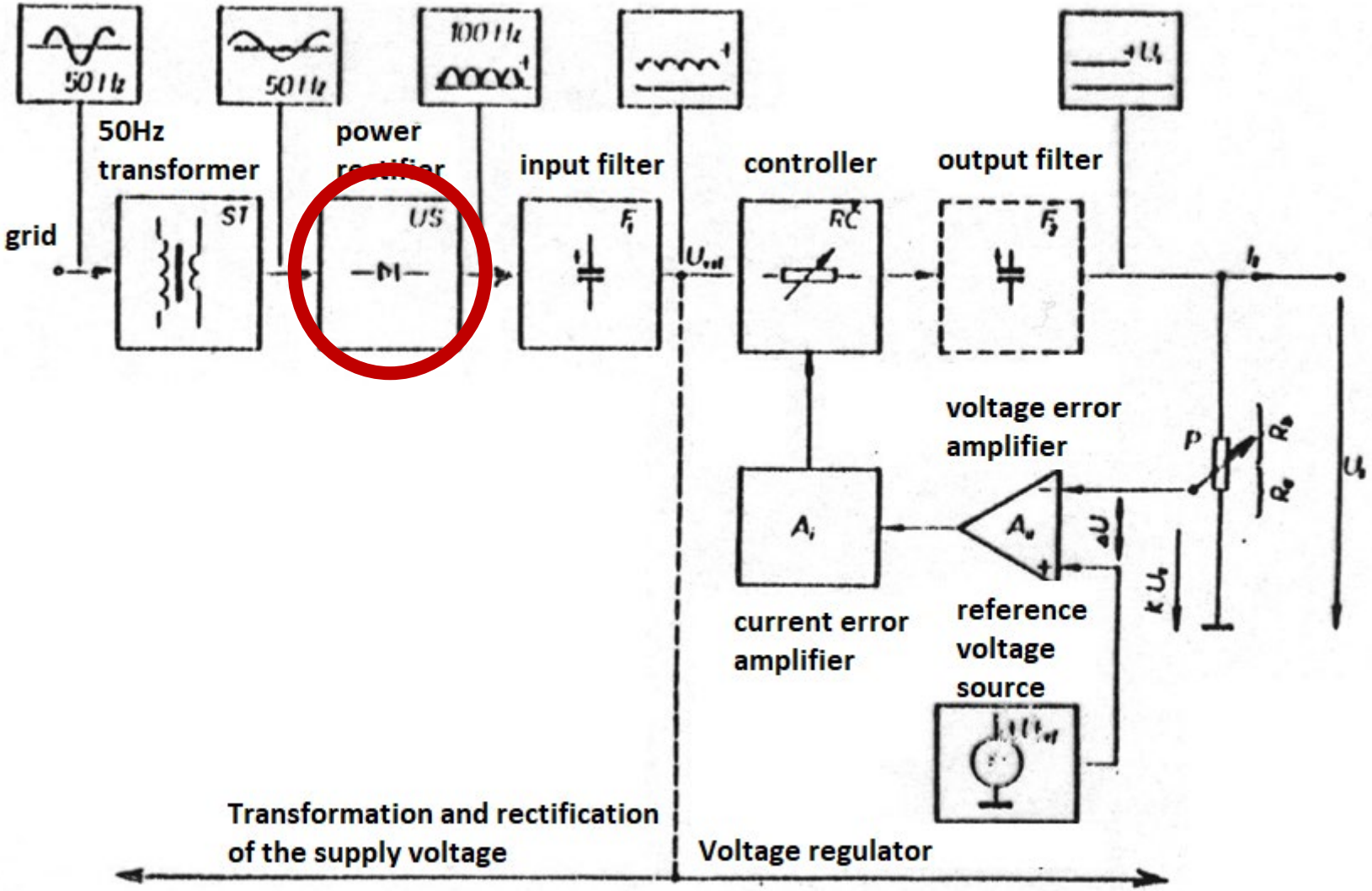
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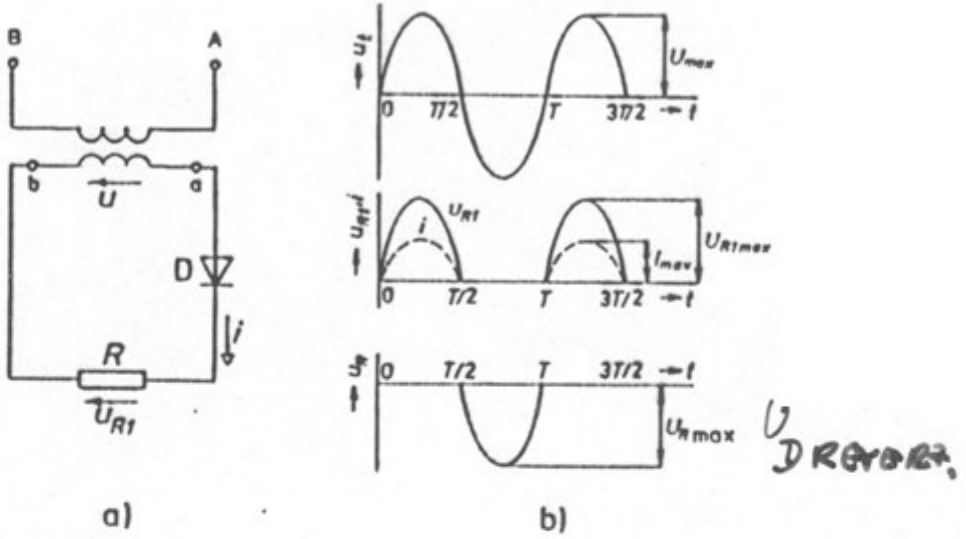
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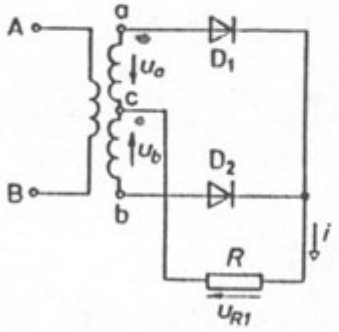


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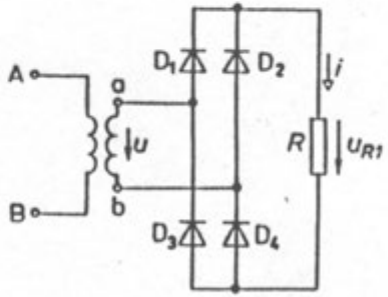
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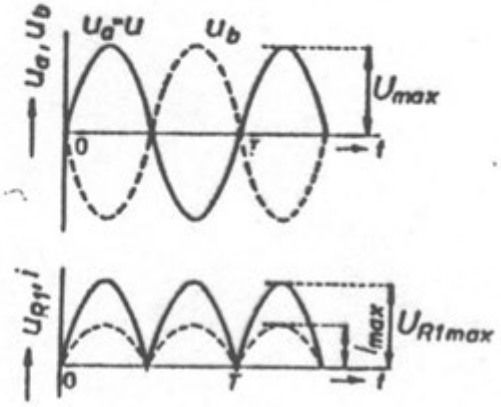
a) b)



obr. x.x Full-wave rectifier using a center tap transformer and 2 diodes

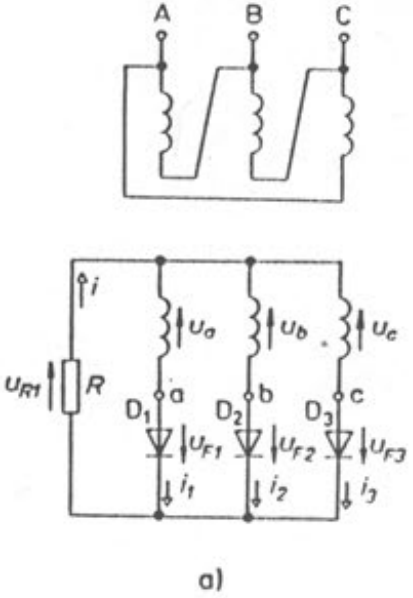


obr.x.x Full-wave rectifier using diode bridge

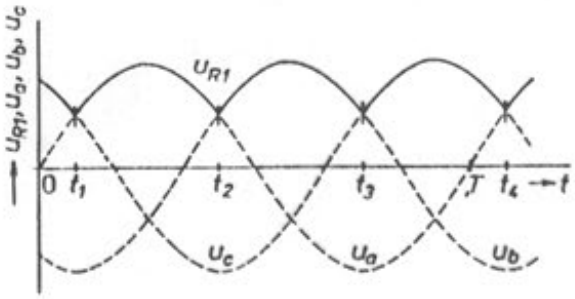


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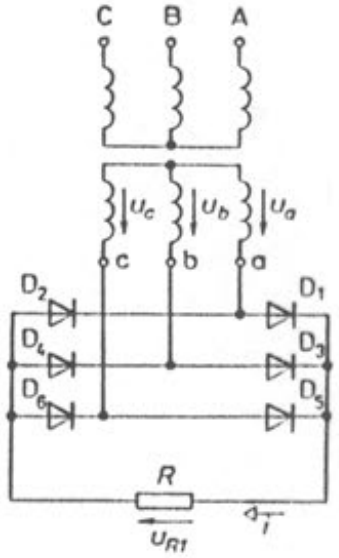
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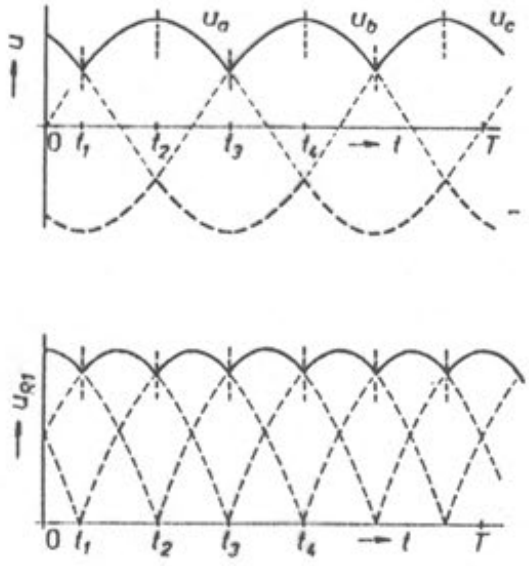
a)



b)



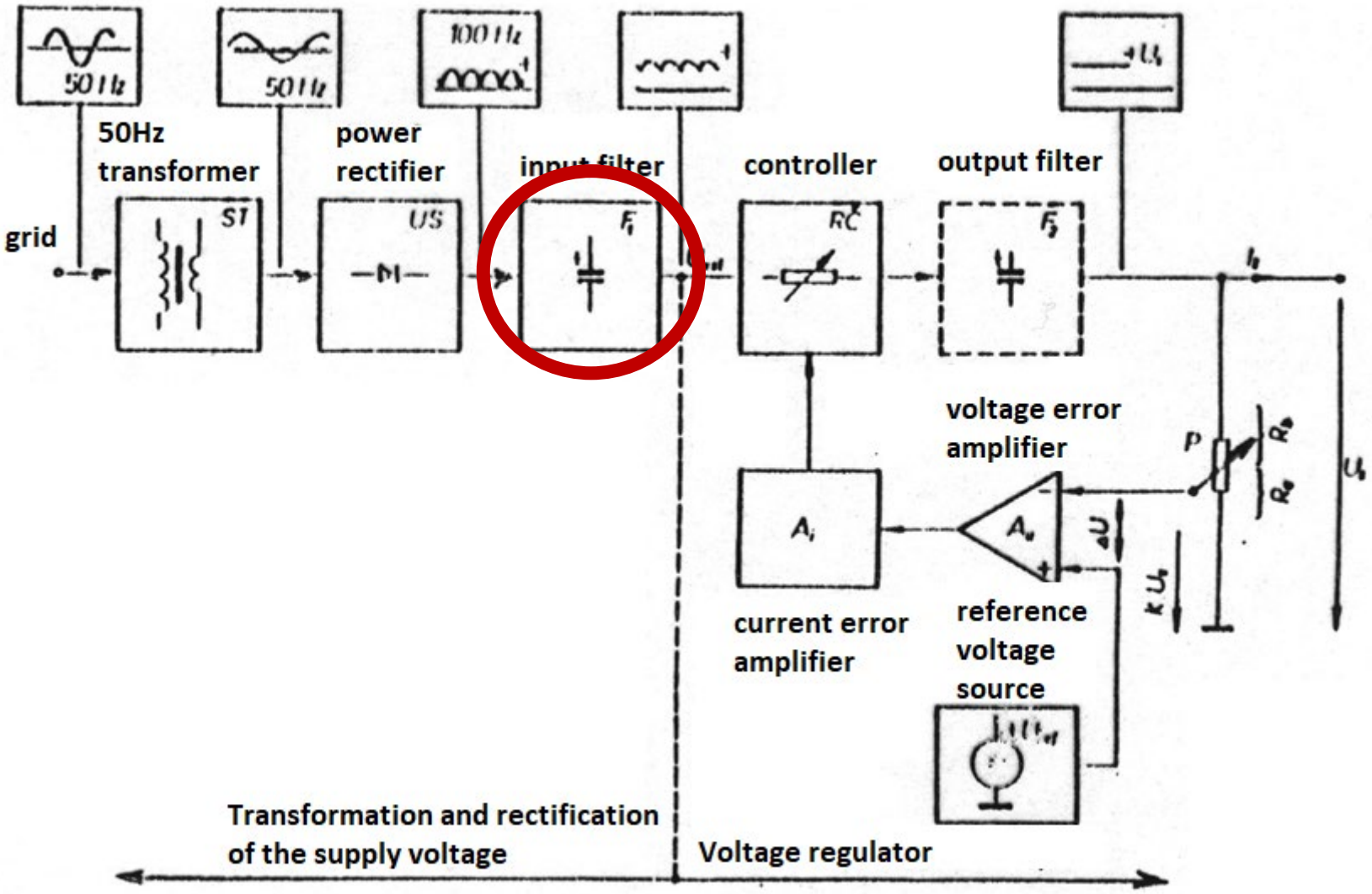
a)



b)

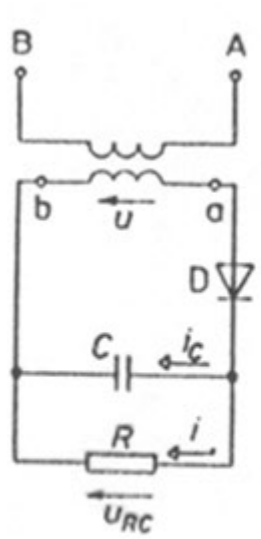
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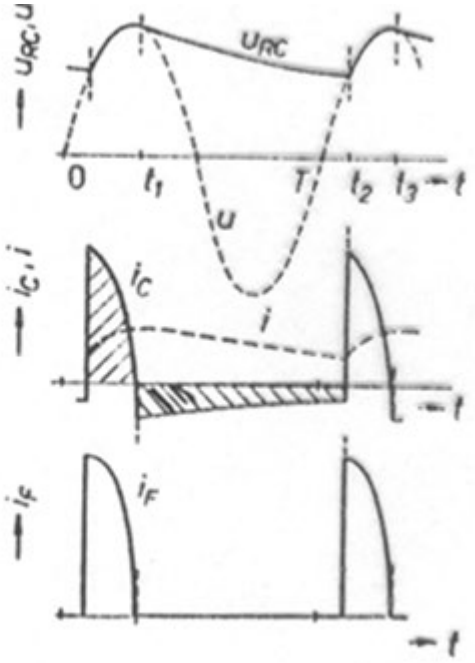
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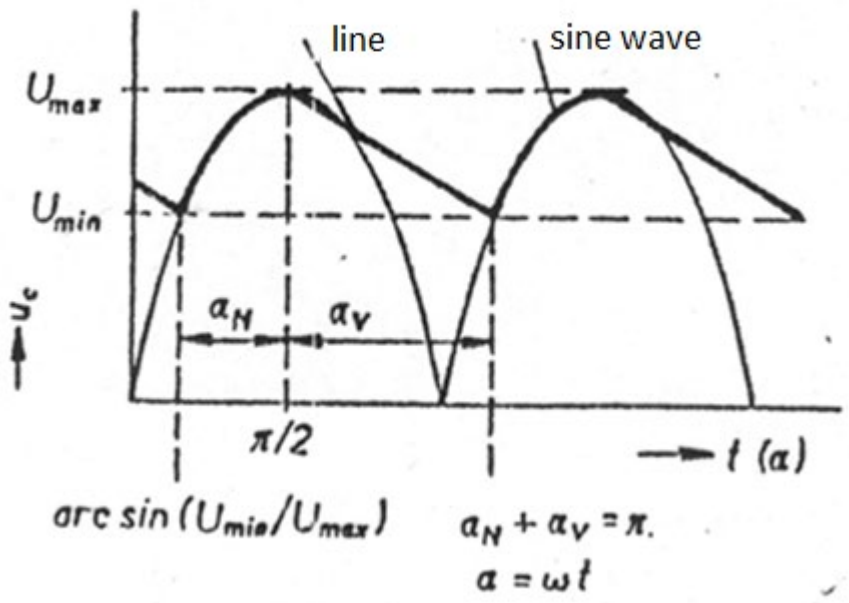


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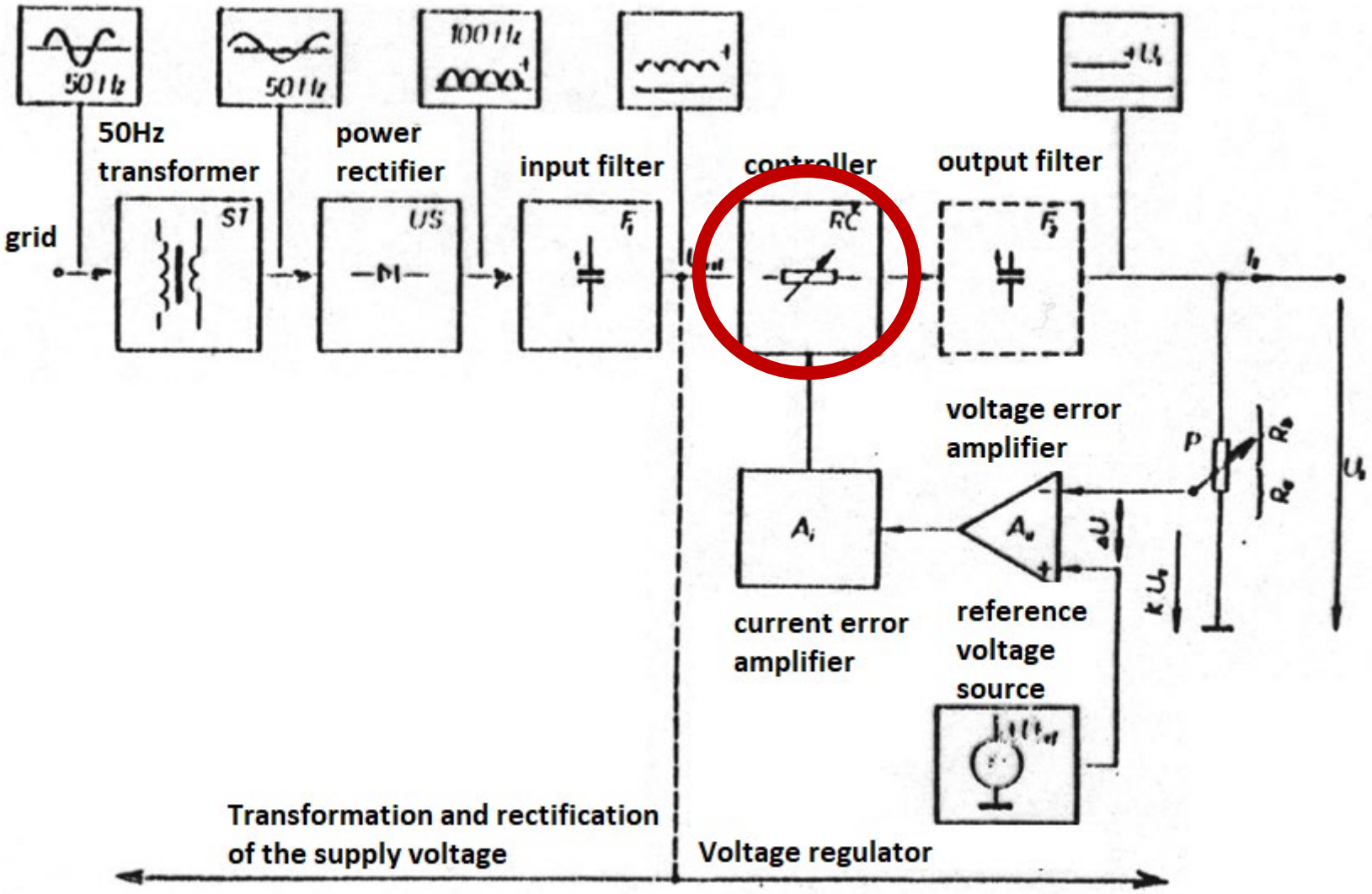






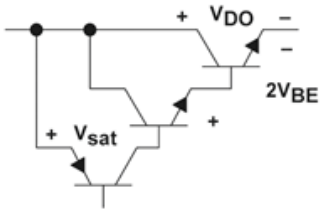
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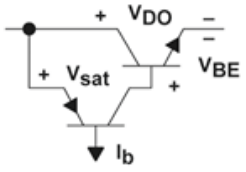
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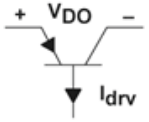
(a) Darlington

$$V_{(dropout)} = V_{CE}(sat) + 2V_{BE} \cong 1.6 \sim 2.5\ V$$ for Darlington



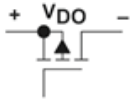
(b) NPN

$$V_{(dropout)} = V_{CE}(sat) + V_{BE} \geq 0.9\ V$$ for NPN regulator



(c) PNP

$$V_{(dropout)} = V_{CE}(sat) \cong 0.15 \sim 0.4\ V$$ for PNP regulator



(d) PMOS

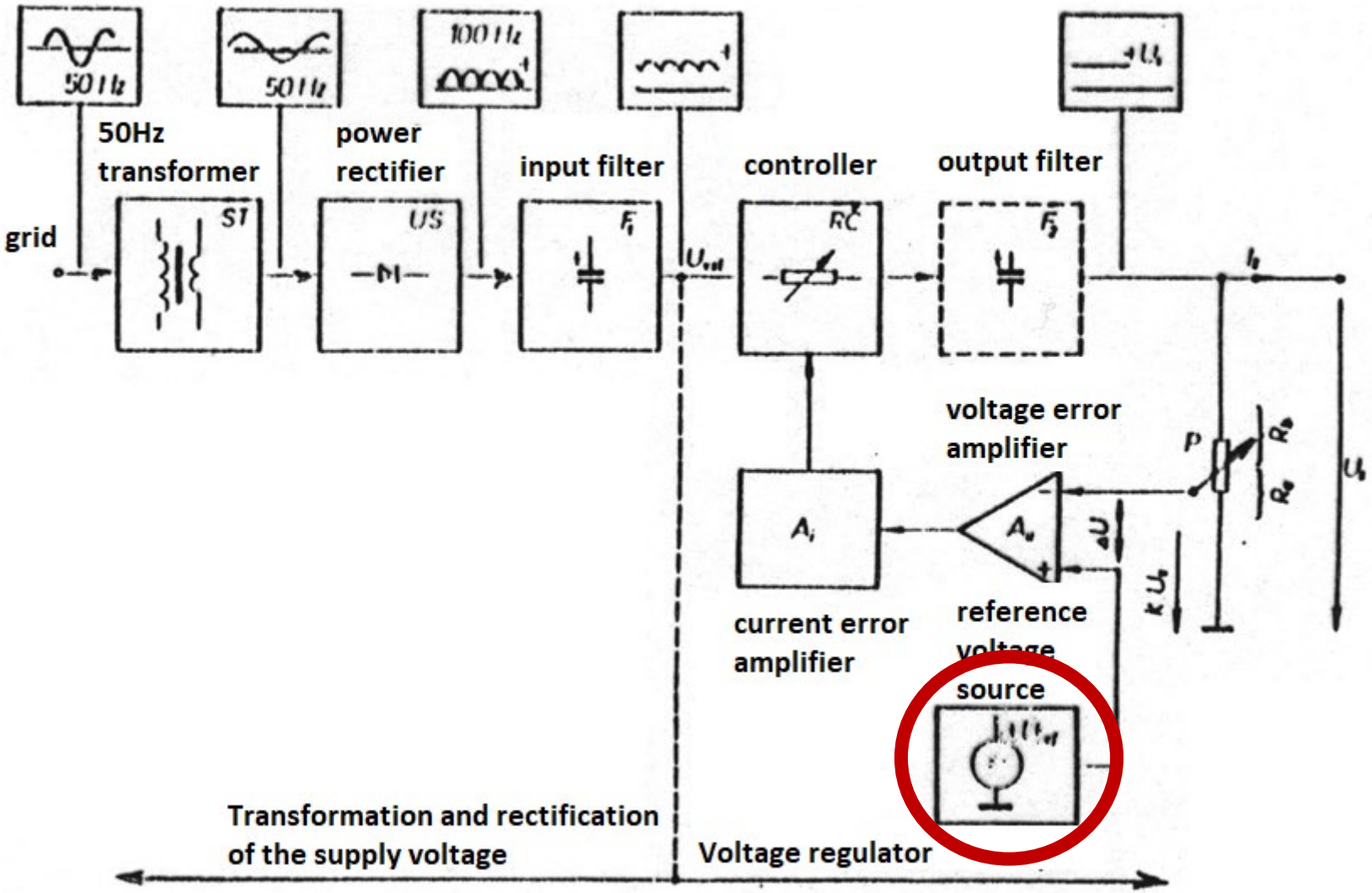
$$V_{(dropout)} = I_o R_{on} \cong 35 \sim 350\ mV$$ for PMOS regulator

Table 1. Comparison of Pass Element Structures

PARAMETER	DARLINGTON	NPN	PNP	NMOS	PMOS
$I_{o,max}$	High	High	High	Medium	Medium
I_q	Medium	Medium	Large	Low	Low
$V_{dropout}$	$V_{sat}+2V_{be}$	$V_{sat}+V_{be}$	$V_{ce(sat)}$	$V_{sat}+V_{gs}$	$V_{SD(sat)}$
Speed	Fast	Fast	Slow	Medium	Medium

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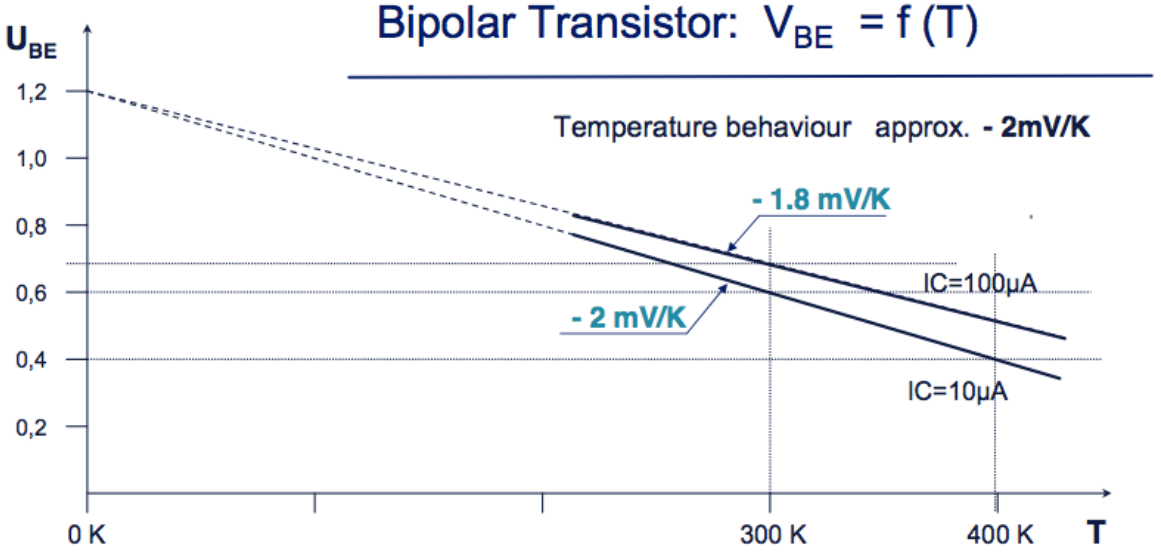
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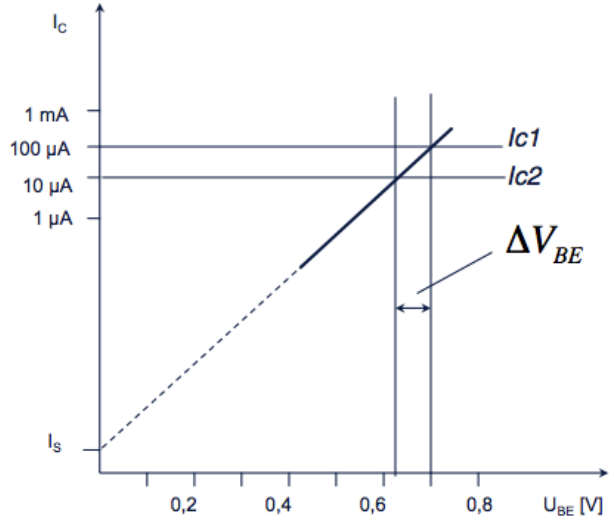


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Bandgap





$$V_{BE} = \ln\left(\frac{I_C}{I_S}\right) \cdot Vt$$

$$\Delta V_{BE} = \ln\left(\frac{I_{C1}}{I_{C2}}\right) \cdot Vt$$

$$Vt = \frac{k \cdot T}{q} \approx 26mV \ [25°C]$$

$$k = 1{,}38 \cdot 10^{-23} \ J/K$$

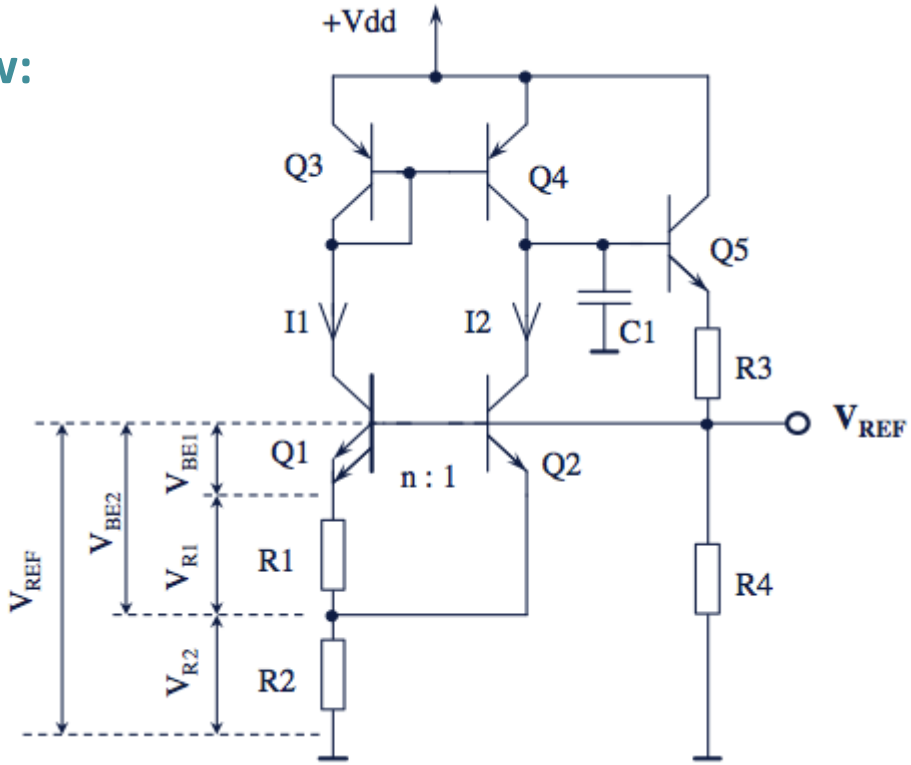
$$q = 1{,}602 \cdot 10^{-19} \ As$$

Respectively:
ΔVbe = Vt·ln(A2/A1)
Δ Vbe = Vt·ln((Ic1/Ic2)(A2/A1))

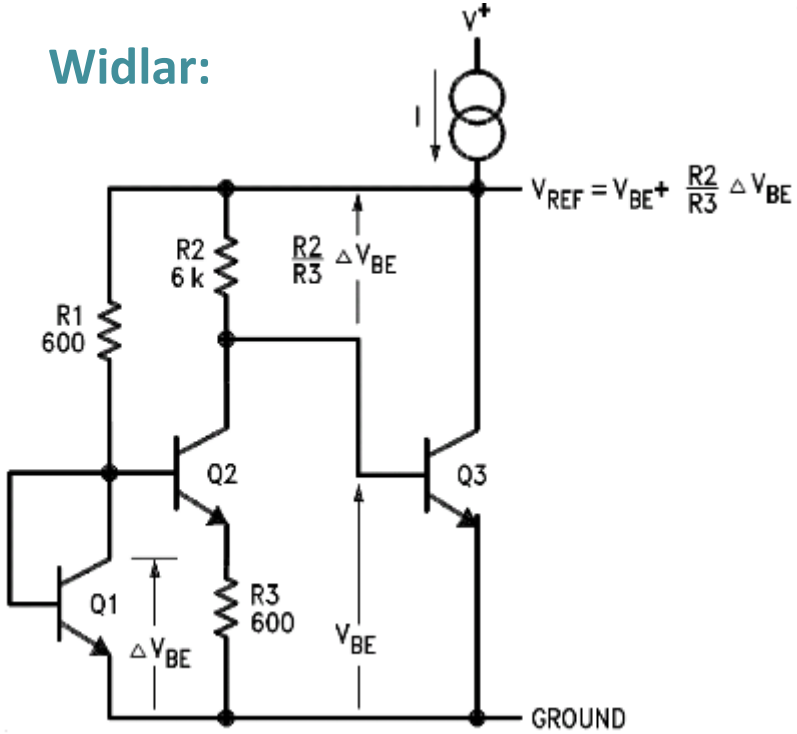
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Brokaw:



Widlar:



$$\Delta V_{BE} = Vt \cdot \ln(n) \qquad n = \frac{AE(Q1)}{AE(Q2)} \qquad Vt = \frac{k}{q} \cdot T$$

$$V_{R1} = \Delta V_{BE} = I_1 \cdot R_1$$

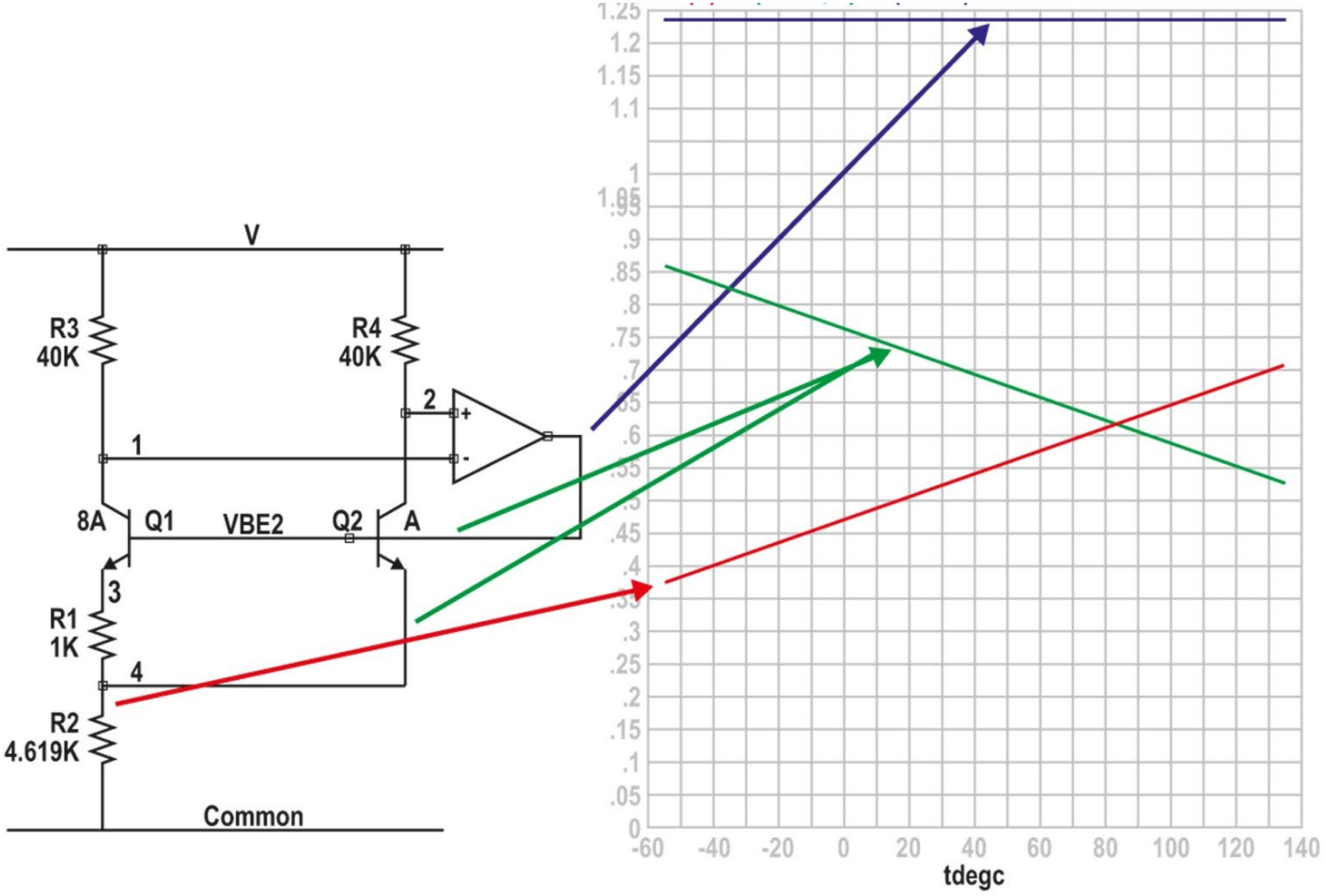
$$V_{R2} = (I_1 + I_2) \cdot R_2 = 2 \cdot I_1 \cdot R_2 = 2 \cdot \frac{R_2}{R_1} \cdot \Delta V_{BE}$$

$$V_{REF} = V_{BE2} + V_{R2} = 1{,}20 \ldots 1{,}25V \quad \textit{for optimal temp .comp .}$$

$$V_{REF} = V_{BE} + \frac{R_2}{R_3} \cdot Vt \cdot \ln\left(\frac{area\,(Q2)}{area\,(Q1)} \cdot \frac{R_2}{R_1}\right)$$

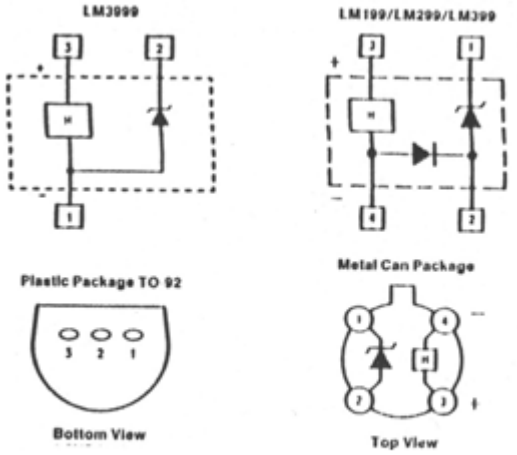
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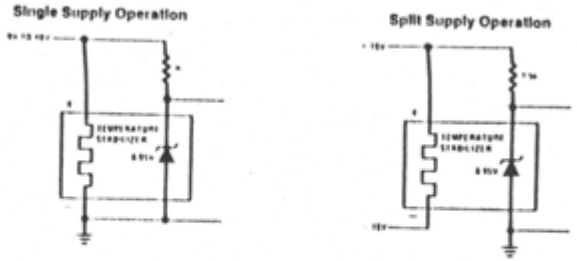


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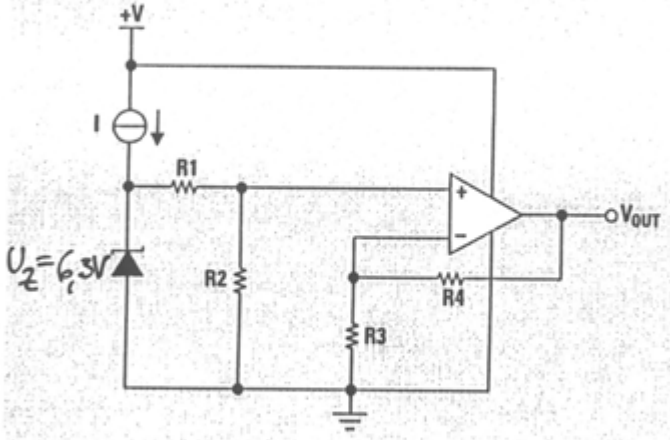


a) Block diagram of LM199



b) LM199 reference voltage circuit

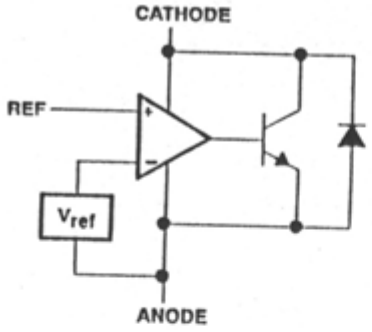
Figure 2. Buried zener reference circuit



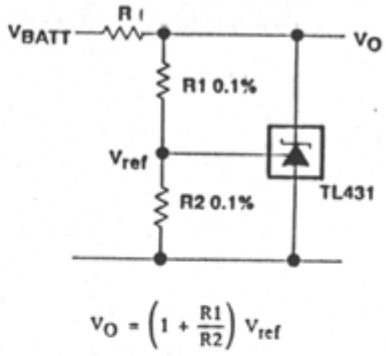
$$V_{OUT} = \frac{U_Z \cdot R_2}{R_1 + R_2} \cdot \left(1 + \frac{R_4}{R_3}\right)$$

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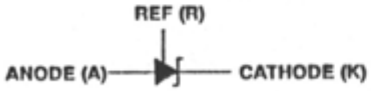
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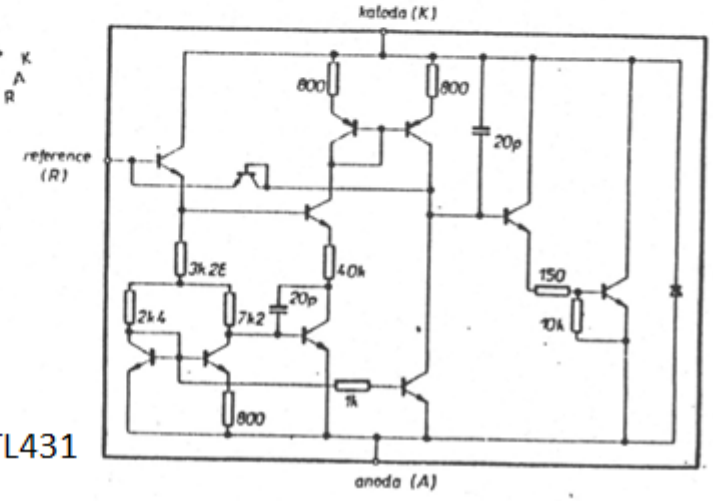
Block diagram of TL431



TL431 circuit





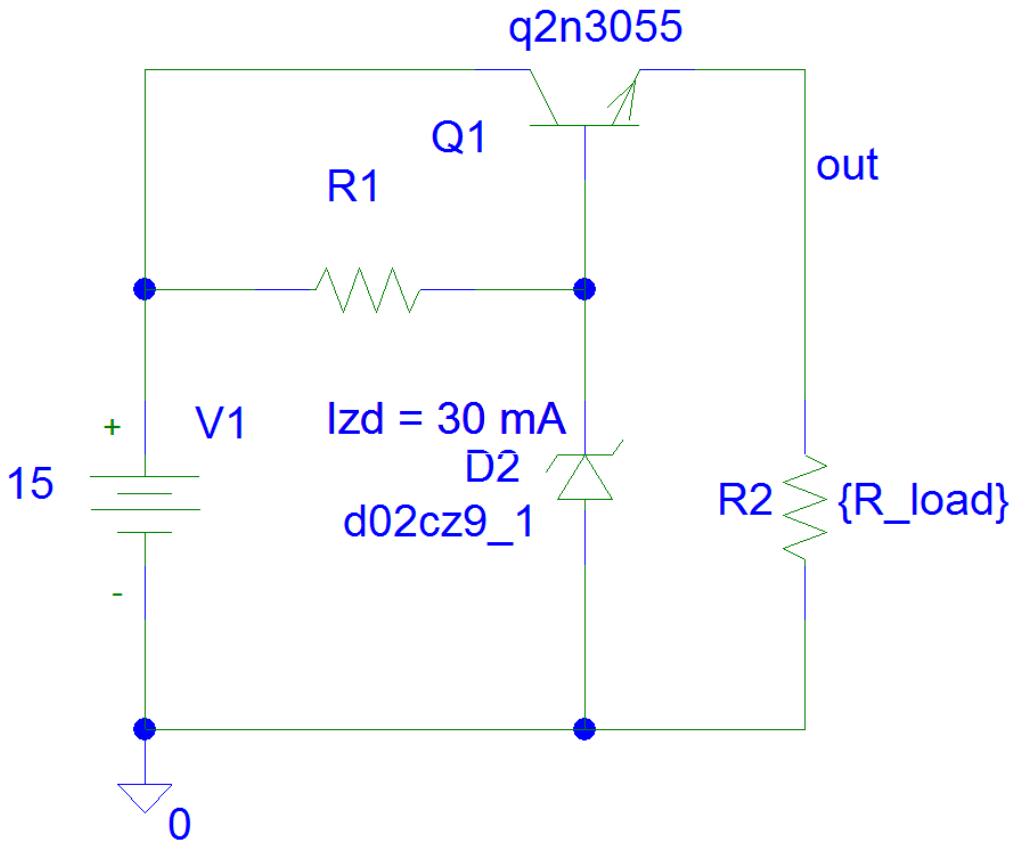


Detailed Schematic of TL431

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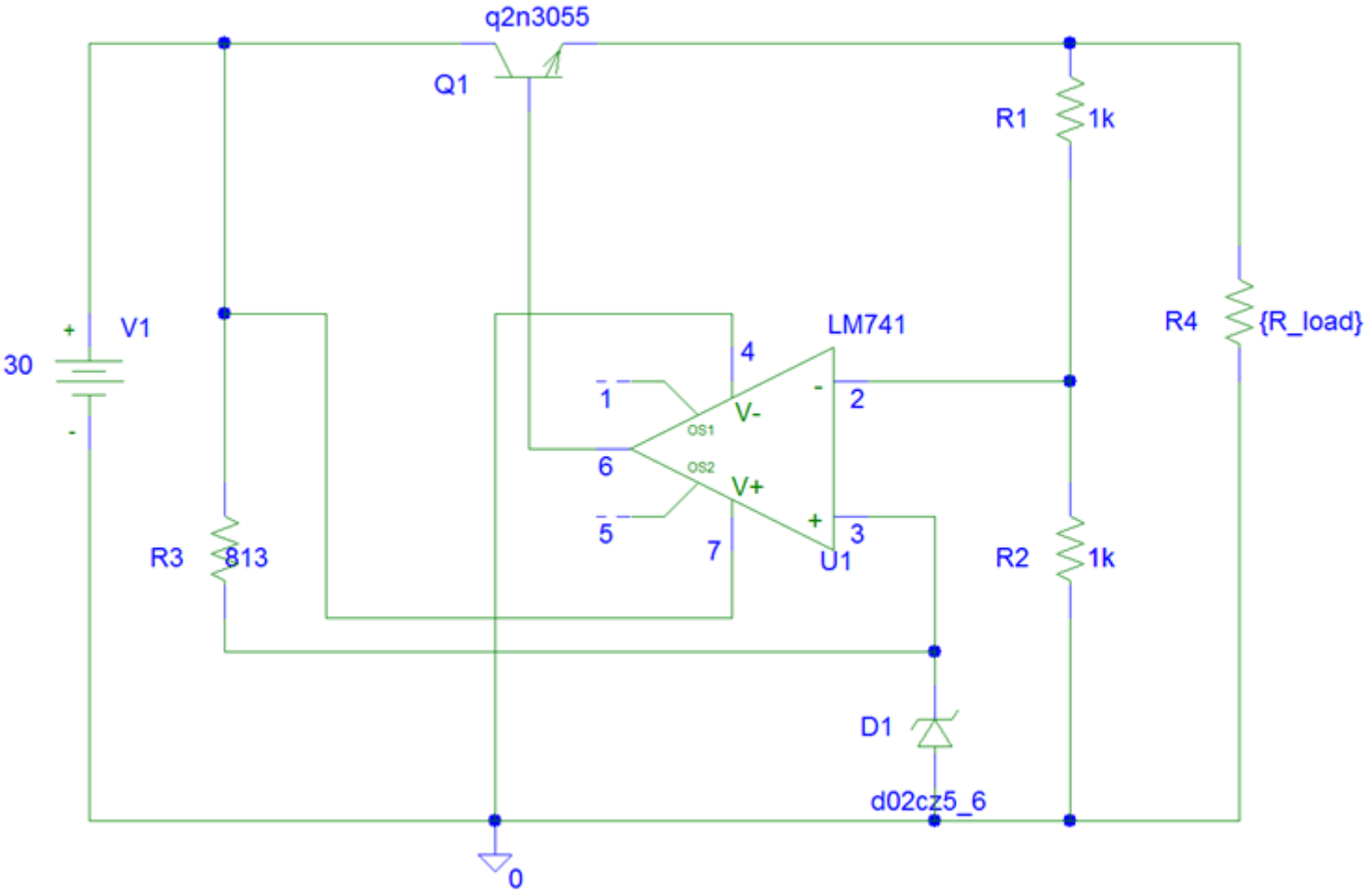
Series regulators



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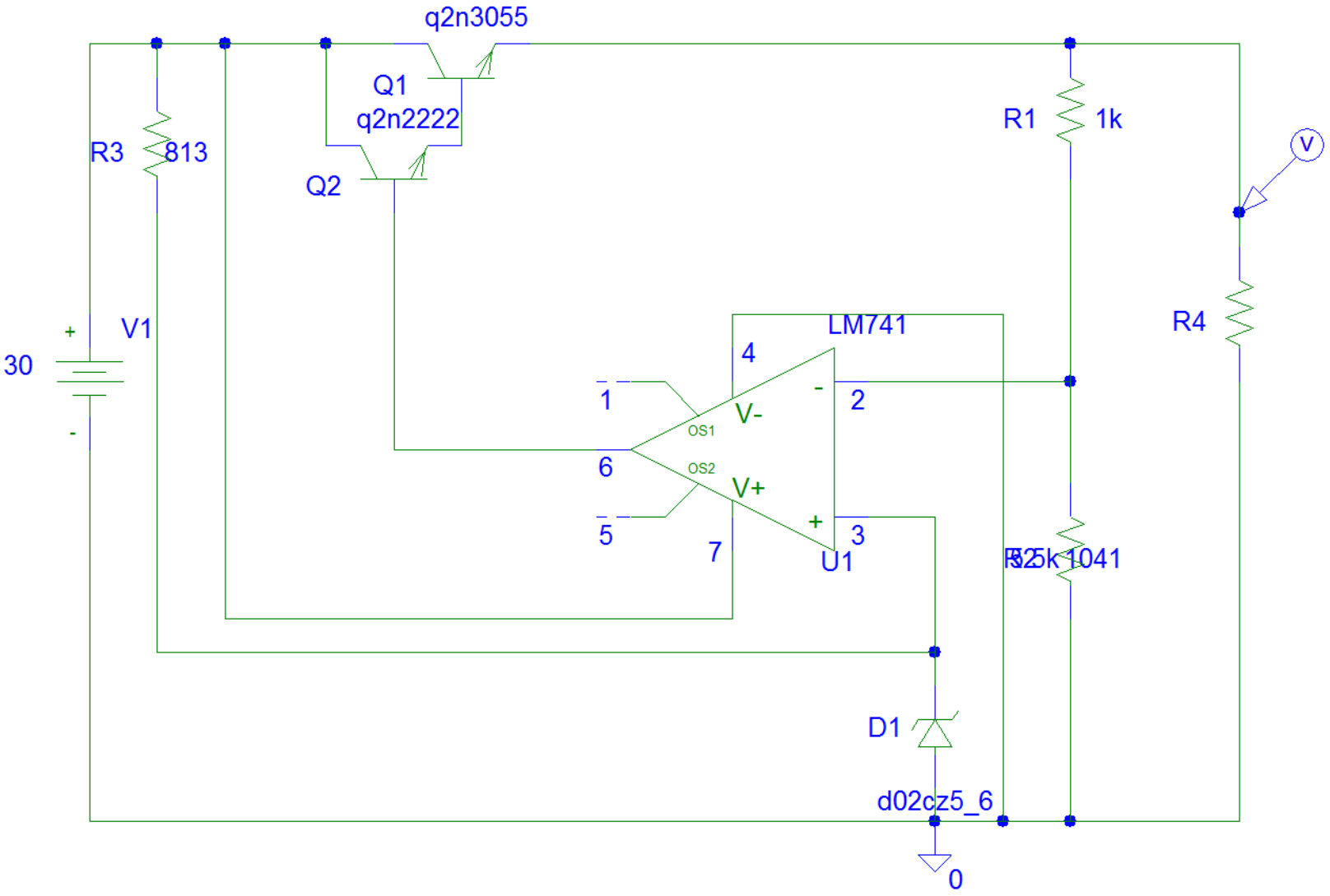
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$$V_{do}=V_{be}+U_{cesat}+(V_{in}-V_{satOZ})$$



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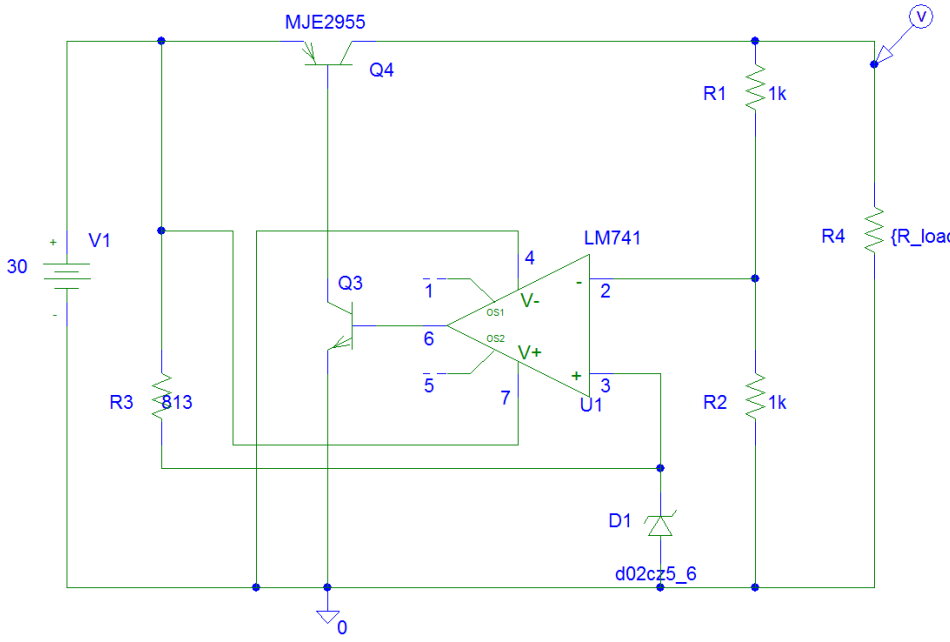
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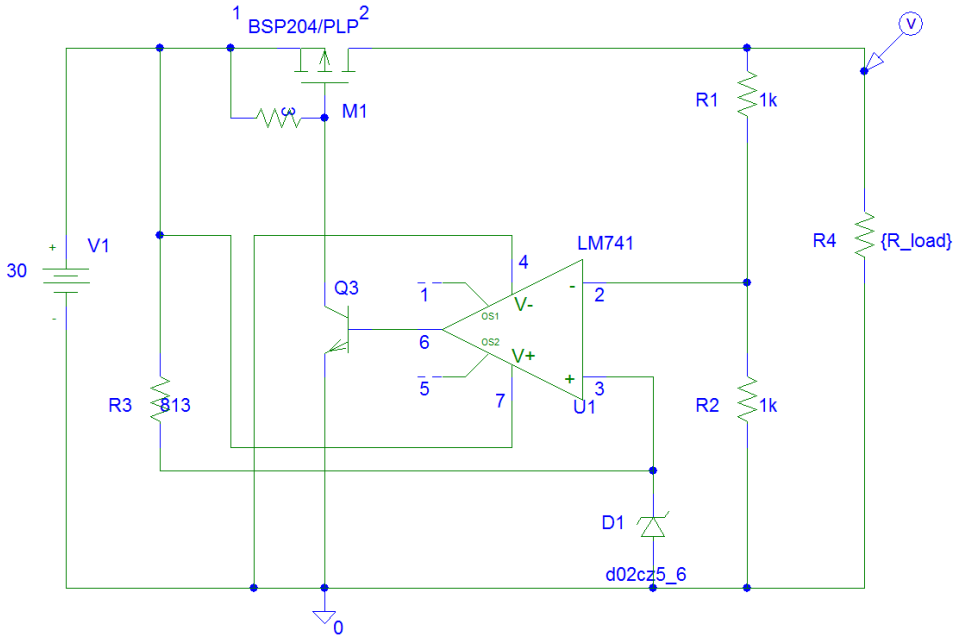


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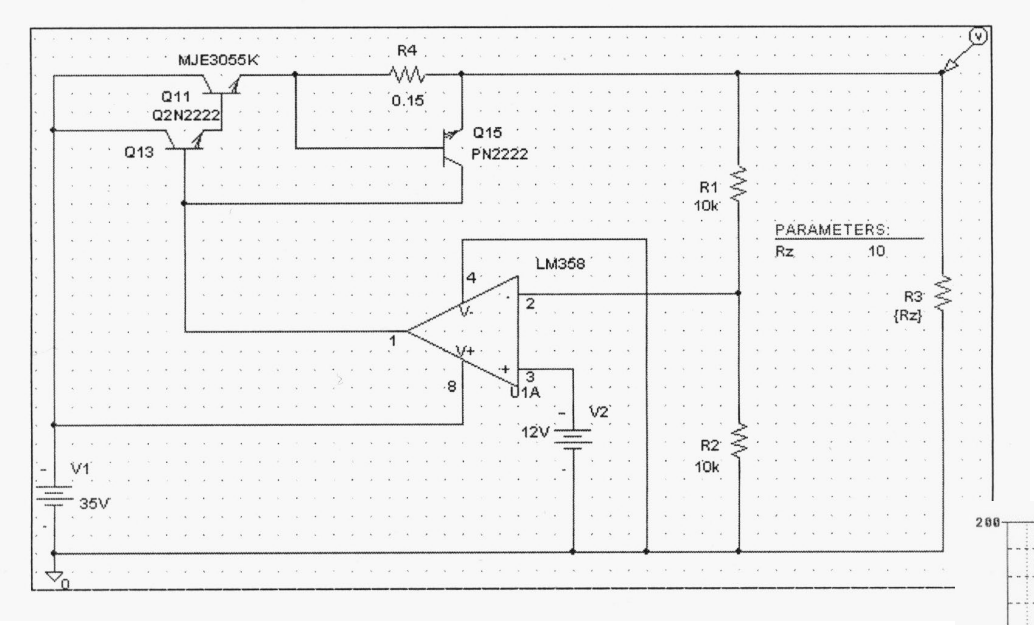


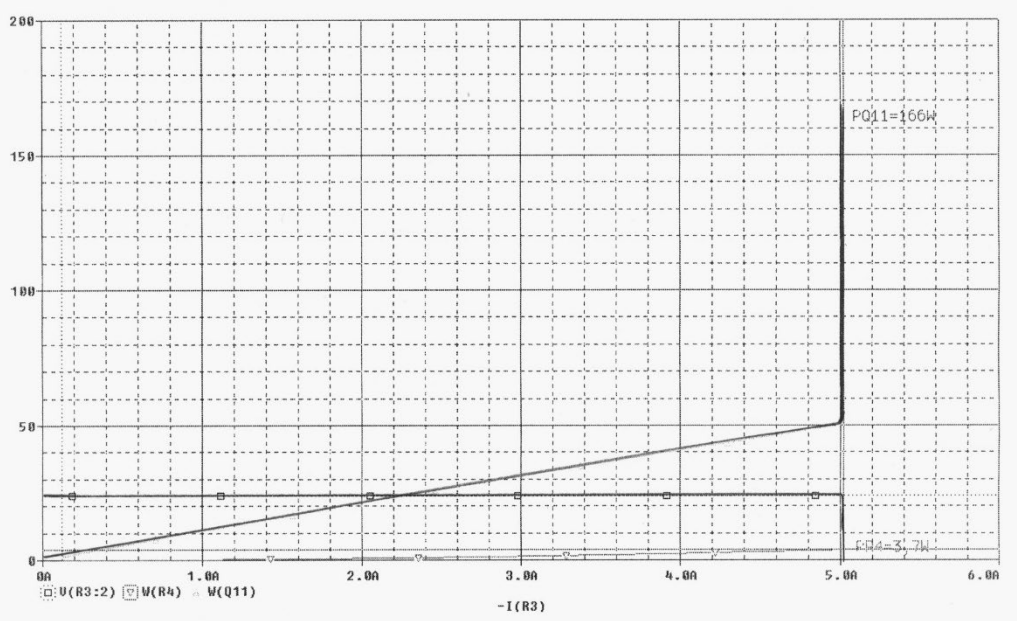


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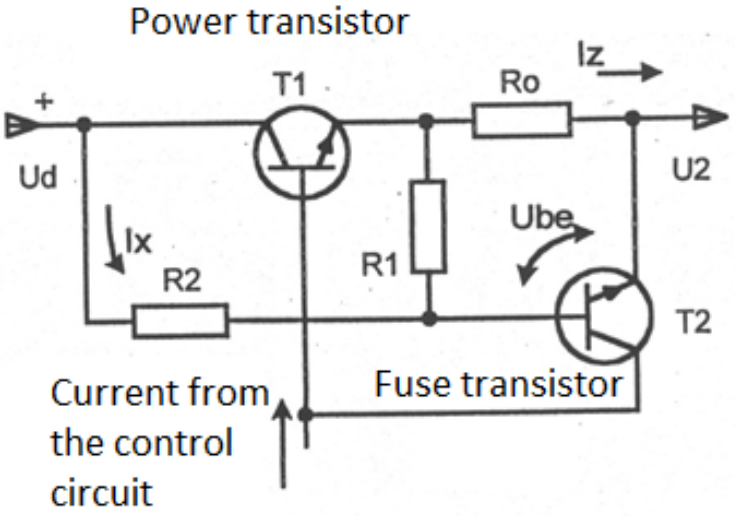
Current limiters





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The following equations are applied to this circuit:

- determination of the maximum current where the protection begins to operate.

Current I_X is the auxiliary current and the following equations apply:

$$I_X = \frac{U_d - U_2}{R_2 + R_1 + R_0}$$

The following applies to the ratios on the BE junction of the transistor T2:

$$0{,}65 = U_{R0} + U_{R1} => 0{,}65 = R_0(I_{Z\,max} + I_X) + R_1 I_X$$

After the modification we get:

$$I_{Z\,max} = \frac{0{,}65}{R_0} - I_X \frac{(R_0 + R_1)}{R_0}$$

- **determination of the minimum current** that is held through a possible short circuit.

Current IX is the auxiliary current under the condition of a short circuit at the output and applies to it the equation:

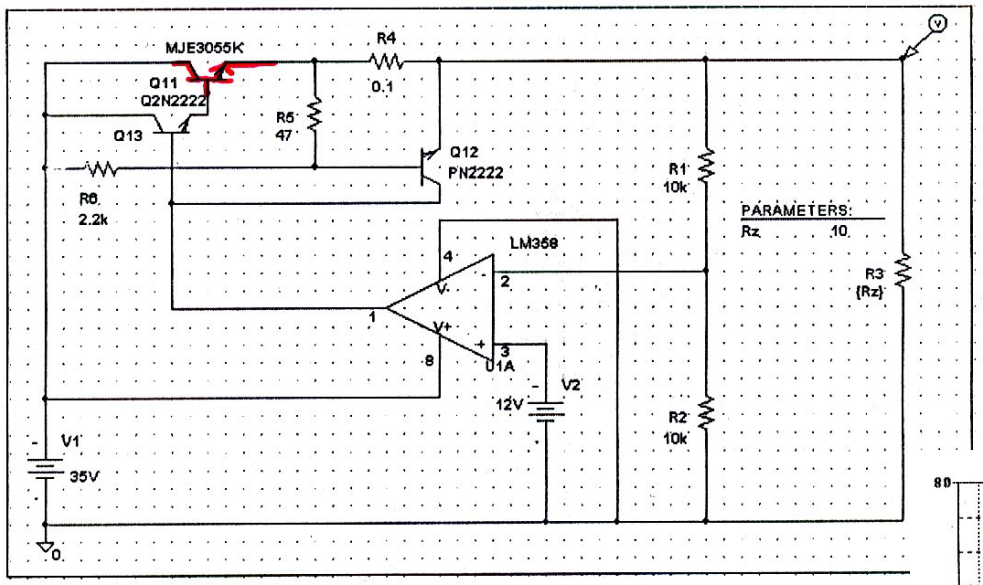
$$I_X = \frac{U_d}{R_2 + R_1 + R_0}$$

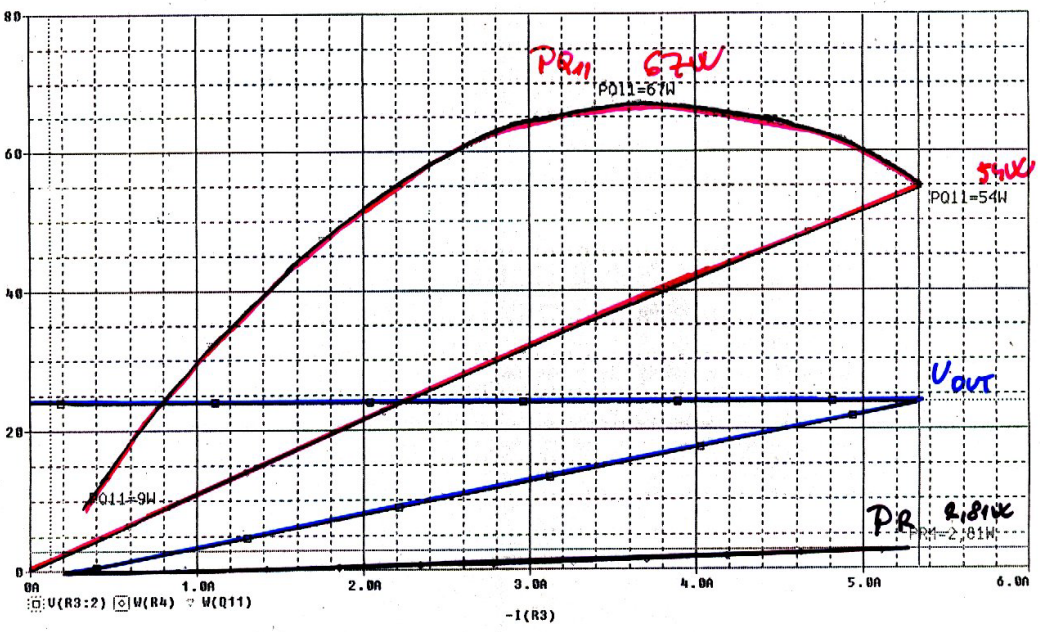
The other equations are the same as in the normal operating state and the relationship for the minimum short-circuit current is given by the equation:

$$I_{Z\,min} = \frac{0{,}65}{R_0} - I_X \frac{(R_0 + R_1)}{R_0}$$

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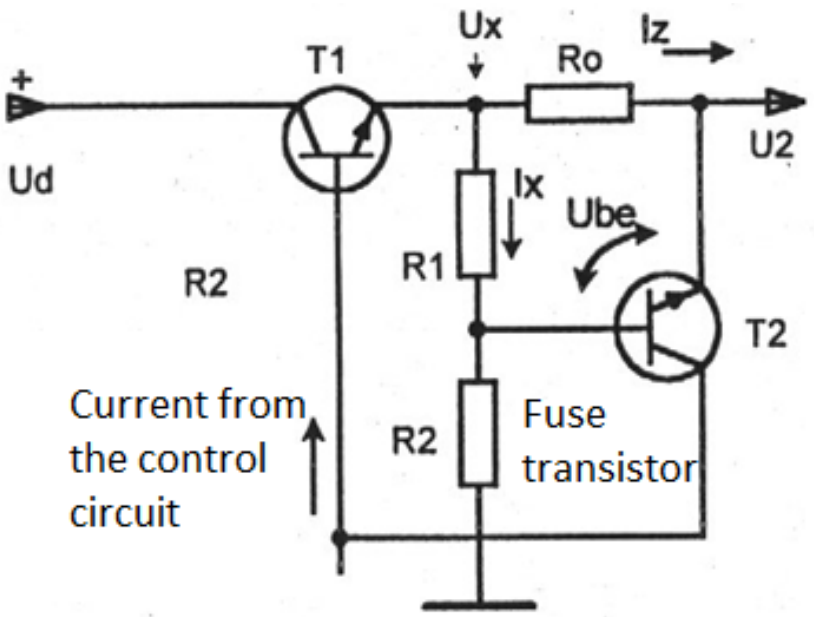
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The following equations apply to this circuit:

- determination of the maximum current at which the protection begins to operate.

$$U_{R0} = R_0 I_{Z\,max}$$

Auxiliary voltage U_x $$U_X = U_2 + R_0 I_{Z\,max}$$

Ratios at R1 $$U_{R1} = \frac{U_X \cdot R_1}{R_1 + R_2}$$

Transistor opening condition $$0{,}65 = U_{R0} - U_{R1}$$

After substituted into the eqn $$0{,}65 = R_0 \cdot I_{Z\,max} - \frac{(U_2 + R_0 \cdot I_{Z\,max}) R_1}{R_1 + R_2}$$

The resulting maximum current $$I_{Z\,max} = \frac{0{,}65 \cdot (R_1 + R_2) + U_2 \cdot R_1}{R_0 \cdot R_2}$$

- determination of the minimum current that is held through a possible short circuit.

$$U_x = R_0 \cdot I_{Z\,min}$$

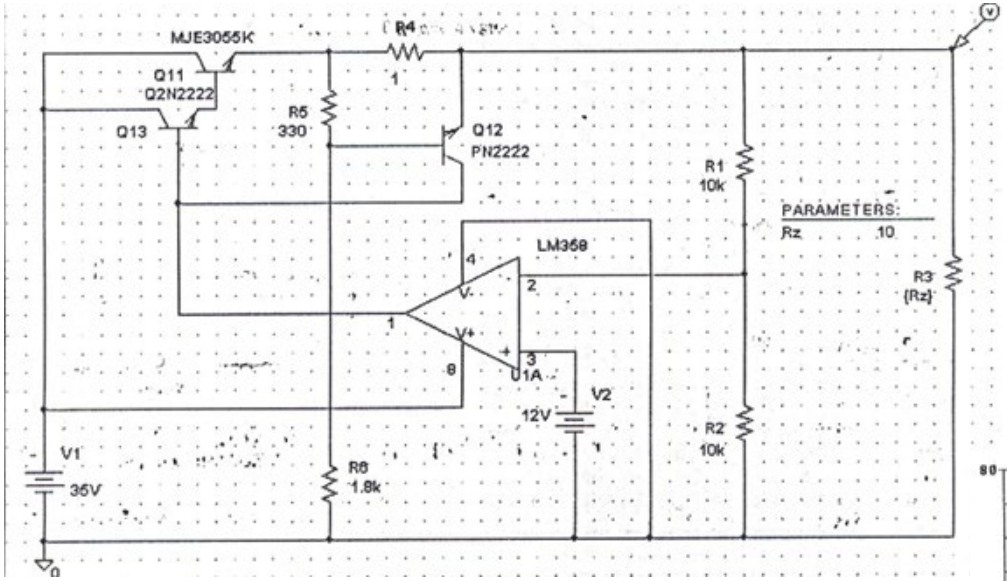
Transistor opening condition: $$0{,}65 = \frac{U_x \cdot R_2}{R_1 + R_2}$$

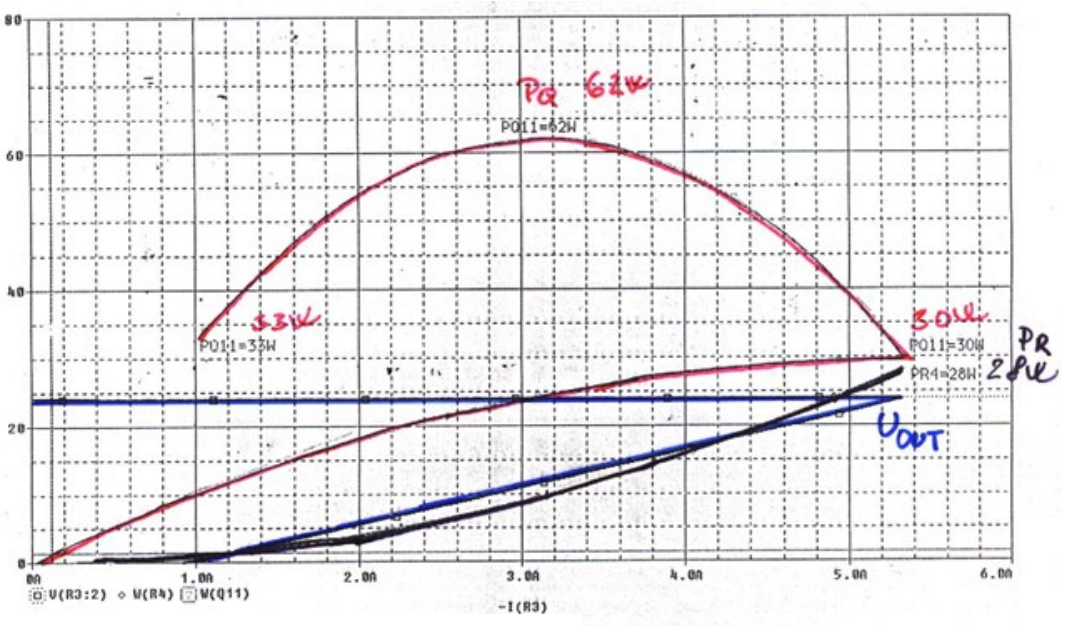
After substituted into the equation $$0{,}65 = \frac{R_0 \cdot I_{Z\,min} \cdot R_2}{R_1 + R_2}$$

The resulting minimum current $$I_{Z\,min} = \frac{0{,}65 \cdot (R_1 + R_2)}{R_0 \cdot R_2}$$

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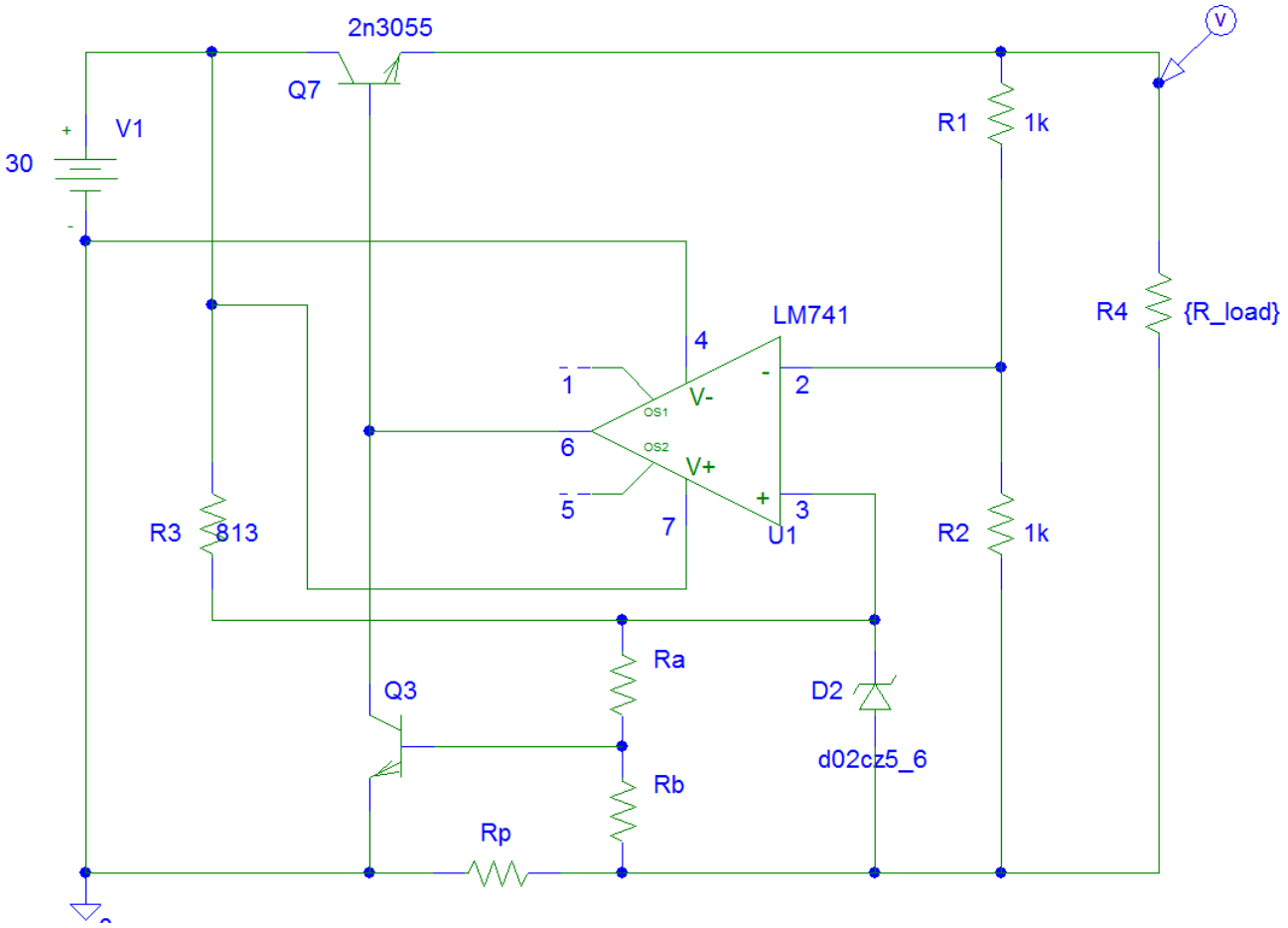
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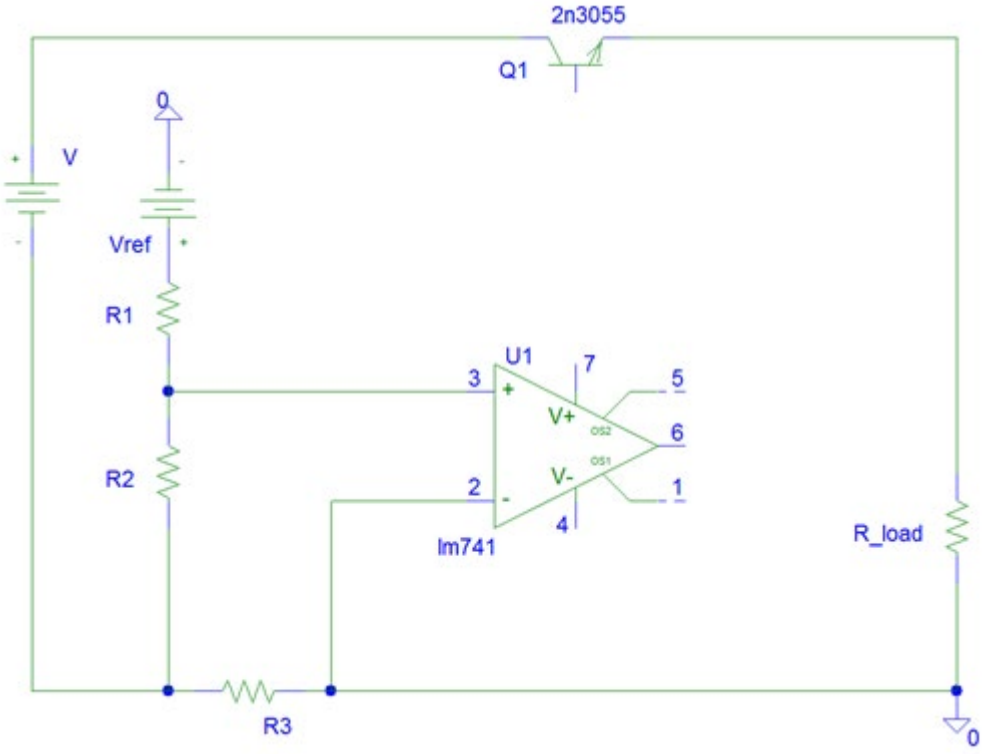
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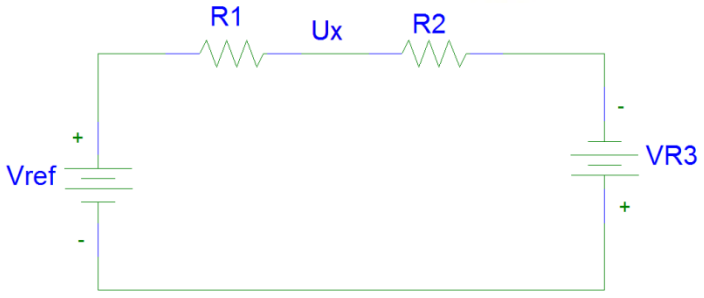


$$V_{beQ3} = V_{Rb} + V_{Rp} \qquad V_{Rb} = V_{ref}\frac{R_b}{R_a + R_b} \qquad V_{Rp} = I_0 \cdot R_p$$

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$$V_{ref} + V_{R3} = V_{R1} + V_{R2}; \qquad I = \frac{V_{ref} + V_{R3}}{R_1 + R_2}$$

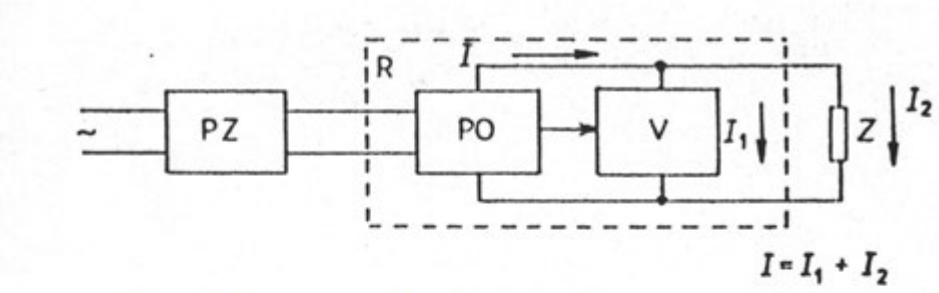
$$V_x = V_{R2} - V_{R3} = V_{ref} + V_{R3}\frac{R_2}{R_1 + R_2}$$

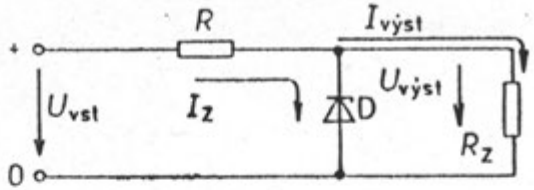
$$0 = V_{ref} R_2 - V_{R3} R_1$$

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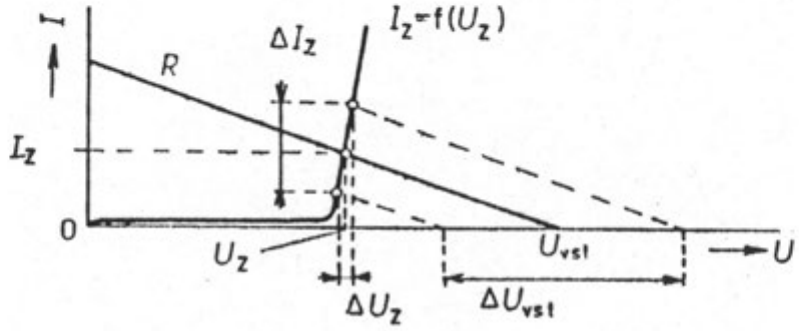
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Shunt regulators



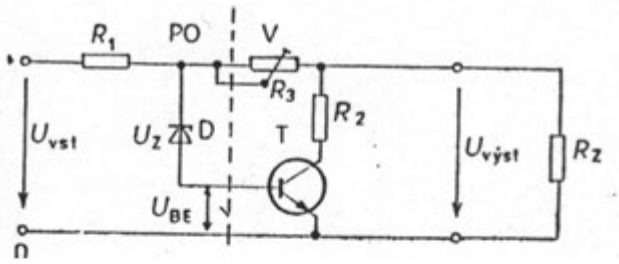


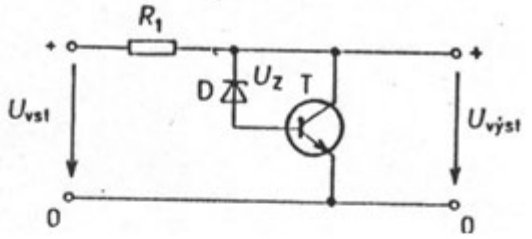
Block diagram of shunt regulator

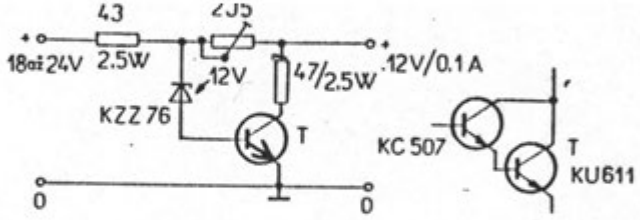


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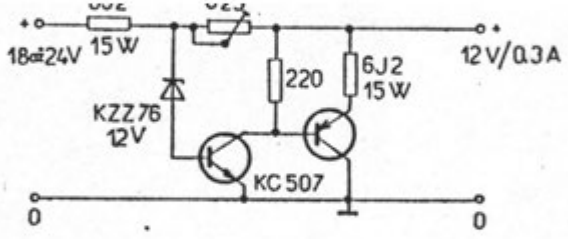
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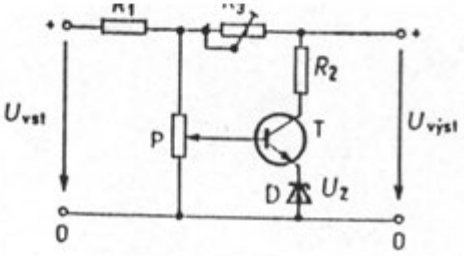




Single-stage regulator



two-stage shunt regulator



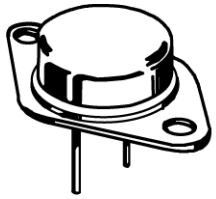
Shunt regulator with
the possibility of adjust
the output voltage

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Transistor parameters

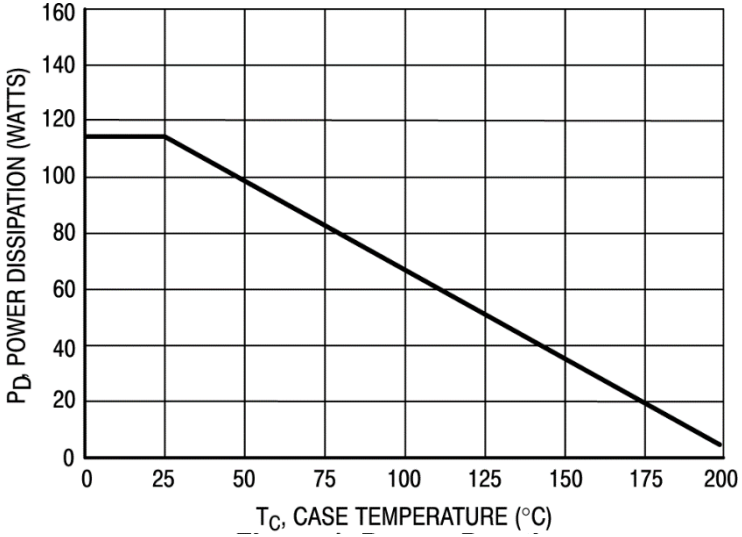
2N3055(NPN)



TO−204AA (TO−3)
CASE 1−07
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Emitter Voltage	V_{CER}	70	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	7	Vdc
Collector Current − Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	115 0.657	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C



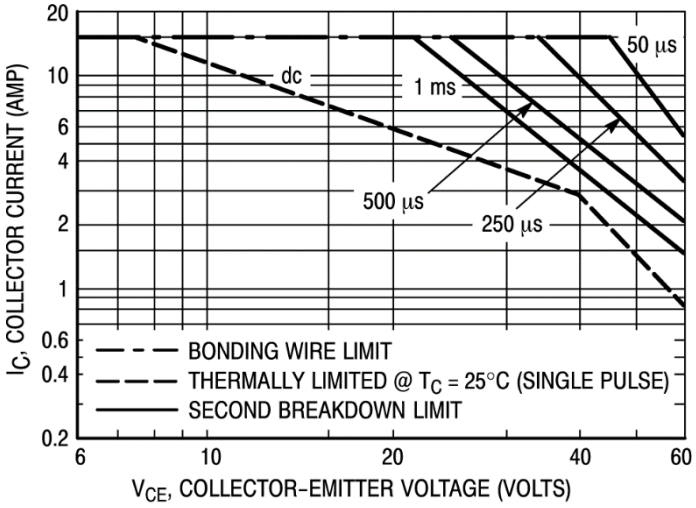


Figure 2. Active Region Safe Operating Area

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Component cooling

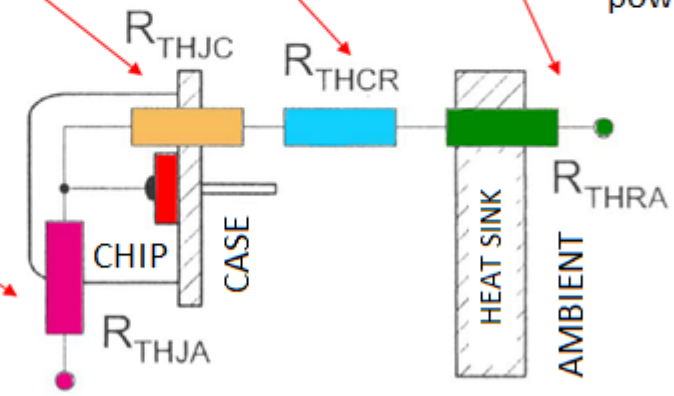
chip temp. υ_j [°C] − ambient temp. υ_a [°C] = (Thermal resistance junction - case. R_{THCJ} [°C/ W] + Thermal resistance case - heatsink (insulating pad) R_{THCR} [°C/ W] + Thermal resistance of the heat sink R_{THRA} [°C/ W]) . Power dissipation of the semiconductor P [W]

P = continuous or average power

R_{THJA} – Thermal resistance junction - ambient

$(R_{THCJ} + R_{THCR} + R_{THRA}) << R_{THJA}$

R_{THCJ} – component parameter specified by the manufacturer



Examples:

KD503 - R_{THCJ} = 0,866 °C/W υ_j = 155°C
2N3055 - R_{THCJ} = 1,5°C/W υ_j = 200°C
2N5686 - R_{THCJ} = 0,584°C/W υ_j = 200°C

Sarkon foil (by type) - R_{THCR} = 0,09 -1,7°C/W

Heatsinks according to design and type of profile - R_{THRA} = 0,1 – 30°C/W

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